**Amendments to the Drawings:**

The attached replacement sheet includes changes to Fig.2. This sheet, which includes Fig.2, replaces the original sheet including Fig.2.

Attachment: Replacement Sheet 1 page(s)

## REMARKS/ARGUMENTS

**Amendments to the specification**

According to the hardware components disclosed in the original claim 1, the specification is amended to fully support the claimed features. No new matter is introduced. Consideration of the amendments to the specification is respectfully requested.

**Amendments to the drawings:**

Fig.2 is amended to include the hardware components disclosed in the original claim 1 and mentioned in the amended paragraph [0017]. No new matter is introduced. Consideration of the amendments to Fig.2 is respectfully requested.

**Amendments to the claims**

Claims 2 & 8 have been amended to properly describe the specific series of microprocessor utilized in the present invention. The acronym MCS has therefore been properly corrected from shorthand notation to refer to Micro Computer System. Micro Computer System is a specific series of microprocessors developed by the Intel Corporation, and is well known to those familiar in the related art. The above claim amendments are fully supported in the original specification paragraph [0004], with no new matter introduced. Applicant respectfully requests consideration of the amendments made to claims 2 and 8.

**Response to Claim Objections**

According to remarks under **Amendments to claims**, claims 2 & 8 have been amended in response to the informalities stated in this Office action.

**Response to Claim Rejections**

**Claims 1-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Zhou et al (5,913,924) (Zhou herein after).**

Applicant asserts that the present invention is not anticipated by Zhou. This is because Zhou does not completely and fully teach the method for accessing a memory with storage space larger than the addressing ability of a microprocessor, as described by the present invention. Further details regarding specific claim rejections are described below.

Regarding claim 1, applicant asserts that Zhou does not teach providing a microprocessor comprising a stack, and a memory bank selector for selecting memory banks. Applicant points out that the memory bank selector is a hardware element that when used in conjunction with the stack, allows for an immediate switching of memory banks. This is in contrast to Zhou, who utilizes a software "space selection instruction...to switch to the first code bank" (Col 6 line 53). Applicant asserts that by virtue of using a space selection instruction, immediate switching of banks is not realized, as a definitive amount of time is required to execute such a code prior to bank switching. Additionally, Zhou teaches use of "a stack (not shown) in data space 350" (Col 6 line 66 ). Verification of Fig. 3 will reveal that data space 350, and hence the stack taught by Zhou, is implemented external to the microprocessor 310. Therefore, applicant asserts that Zhou does not teach a microprocessor comprising a stack and a memory bank selector as disclosed in claim 1 of the present invention.

Furthermore, use of the stack and memory bank selector as taught in the present invention allow for better optimization and allocation of memory when compared to the teachings of Zhou. Because Zhou alternatively utilizes a space selection instruction for bank switching, a space selection instruction is required in every memory bank (space selection instructions 375A/B, Figs. 3,4). This contrasts the present invention, as space selection instructions are not required, allowing optimized usage of available memory banks (see Fig. 2).

Additionally, applicant points out that Zhou does not teach pushing a bank number of the current memory bank onto the stack, as disclosed in the limitation for step (b) of claim 1. Examiner has provided references of (Col 6, lines 65-67) which states "Microprocessor 310 saves the next address aaa1 on a stack in data space 350" and (Col 7, lines 10-37) stating "microprocessor 310 switches banks to retrieve and execute instructions...a space selection instruction at address bbb2 that switches execution to code bank 370A". Neither of the provided references explicitly disclose the pushing of a bank number onto a stack. Therefore, Zhou does not utilize a stack to store a bank number of the current memory bank as taught by the present invention, but only to store the next address in the operational program code.

Under the same rationale, Zhou also cannot teach popping the bank number of the memory bank stored in step (b) from the stack, as disclosed in step (d) of claim 1of the present invention. Because Zhou does not teach initially storing a bank number of the current memory bank by pushing it onto the stack as described above, applicant points out that popping the bank number cannot occur.

In summary, applicant asserts that Zhou does not teach providing a microprocessor comprising a stack, and a memory bank selector for selecting memory banks. Zhou alternatively uses a "space selection instruction...to switch to the first code bank" (Col 6 line 53), and for general bank switching, where a space selection instruction is required in every memory bank (see space selection instructions 375A/B, Figs. 3,4). This requires additional memory consumption when compared to the method of the present invention (Fig. 2). Additionally, Zhou does not teach pushing a bank number of the current memory bank onto the stack, as the stack of Zhou is alternatively used for "saves the next address aaa1 on a stack in data space 350" (Col 6, lines 65-67). For at least the above mentioned reasons, applicant kindly requests the Examiner re-evaluate claim 1 in reconsideration for its allowance.

Regarding claim 2, applicant points out that Zhou does not teach the microprocessor being a Micro Computer System (MCS) series processor. Zhou teaches "Microprocessor system 300 includes a microprocessor 310, such as Zilog

Z80" (Col 4 line 37). Those familiar in the art are aware that the MCS is an Intel produced processor, having a different architecture and instruction set than the Zilog produced Z80. Therefore, applicant points out that the teachings of Zhou may not be applicable to an MCS processor, as disclosed in claim 2 of the present invention. In addition, since claim 2 is dependent upon claim 1, it should be allowed if claim 1 is found allowable. Reconsideration of claim 2 is respectfully requested.

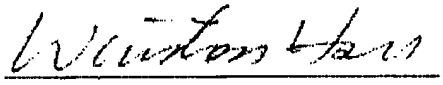
Regarding claims 3-5, applicant asserts that these claims are dependant upon claim 1. Therefore, if an allowance is made for claim 1, applicant asserts that similarly, allowances should be made for claims 3-5 as being dependant on claim 1. Reconsideration of claims 3-5 is respectfully requested.

Regarding claim 7, please see above arguments made for claim 1, as claim 7 is an analogous hardware claim to the method disclosed in claim 1. Particularly, applicant asserts that Zhou does not teach the microprocessor for pushing onto a stack a bank number of a current memory bank upon the interrupt. Again, a similar rationale follows as that described for claim 1. Reconsideration of claim 7 is respectfully requested.

Regarding claim 8, please see above arguments made for claim 2. Reconsideration of claim 8 is respectfully requested.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Sincerely yours,



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Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 12 hours behind the Taiwan time, i.e. 9 AM in D.C. = 9 PM in Taiwan.)